REMARKS

The Examiner rejected claim 34 under 35 U.S.C. § 112, second paragraph.

The Examiner rejected claim 34-36 under 35 U.S.C. § 103(a) as allegedly being unpatentable over US Patent Number 6,674,971 to Boggess *et al.*, in view of US Patent Application Publication Number 2004/0215929 to Floyd *et al.*

The Examiner rejected claim 43 under 35 U.S.C. § 103(a) as allegedly being unpatentable over US Patent Number 6,674,971 to Boggess *et al.*, in view of US Patent Application Publication Number 2004/0215929 to Floyd *et al.*, as applied to claim 34 above, and further in view of US Patent Number 6,081,527 to Chappel *et al.*

The Examiner rejected claim 37 under 35 U.S.C. § 103(a) as allegedly being unpatentable over US Patent Number 6,674,971 to Boggess *et al.*, in view of US Patent Application Publication Number 2004/0215929 to Floyd *et al.*, as applied to claim 34 above, and further in view of US Patent Number 4,797,879 to Habbab *et al.*

The Examiner rejected claim 38-42 under 35 U.S.C. § 103(a) as allegedly being unpatentable over US Patent Number 6,674,971 to Boggess *et al.*, in view of US Patent Application Publication Number 2004/0215929 to Floyd *et al.*, as applied to claim 34 above, and further in view of US Patent Number 5,946,116 to Wu *et al.*

Applicants respectfully traverse the § 112 and § 103 rejections with the following arguments.

35 U.S.C. § 112, Second Paragraph

The Examiner rejected claim 34 under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The Examiner suggests: "Appropriate corrections in the claim language for claim 34, lines 1-8 is suggested below: 34. An optical transmission method, comprising:

sending an address of a second core and control signals from a first core to a first optic controller in an integrated circuit, said integrated circuit comprises:

the first core,

the first optic controller connected to the first core,

a plurality of optical transmitters under control of the first optic controller,

the second core,

a second optic controller connected to the second core,

a plurality of optical receivers under control of the second optic controller, and

a plurality of optical channels, wherein each optical channel extends from one of the optical transmitters to one of the optical receivers;"

In response, Applicants have amended claim 34 in accordance with the preceding suggestion by the examiner.

35 U.S.C. § 103(a)

The Examiner rejected claim 34-36 under 35 U.S.C. § 103(a) as allegedly being unpatentable over US Patent Number 6,674,971 to Boggess *et al.*, in view of US Patent Application Publication Number 2004/0215929 to Floyd *et al.*

Applicants respectfully contend that claim 34 is not unpatentable over Boggess in view of Floyd, because Boggess in view of Floyd does not teach or suggest each and every feature of claim 34.

As a first example of why claim 34 is not unpatentable over Boggess in view of Floyd, Boggess Boggess in view of Floyd does not teach or suggest the feature: "sending **an address** of a second core and control signals from a first core to a first optic controller" (emphasis added).

The Examiner argues that in FIG. 6A of Boggess, the CPU 200 and the gate controller 210 respectively represent the first core and the first optic controller of claim 34.

In response Applicants respectfully contend that Boggess does not teach or suggest that the CPU 200 sends **an address** of a second core to the gate controller 210. To the contrary, Boggess teaches that a feature of Boggess' invention is that said address is not needed. See Boggess, col. 9, lines 46-48 ("A further object is a method of communicating on a network, wherein the step of passing through the optical data is done **without reading a destination address**. "). See also, Boggess, col. 10, lines 58-59 ("it is no longer necessary to include addressing information in data streams"). See also, Boggess, col. 15, lines 34-36 ("the addressing information is determined by the channel being used and not by the destination address information in the header").

In "Response to Arguments", the Examiner argues that "Applicant cited Boggess col 15, lines 34-36 ("the addressing information is determined by the channel being used and not by the

destination address information in the header"). Therefore, the address of a second core is in fact being sent in a form of channel being used, since each channel represents a specific address."

In response, Applicants assert that Boggess, col. 15, lines 34-36 does not teach or suggest that "a channel being used"is sent, as an address of a second core, from the CPU 200 (alleged by the Examiner to be the first core) to the gate controller 210 (alleged by the Examiner to be the first optic controller), as required by the language of claim 34. There is absolutely no disclosure in Boggess of sending an address of a second core from the CPU 200 to the gate controller 210.

In addition, the Examiner alleges that the CPU in node 2 of Boggess, FIG. 7A as the second core of claim 34. However, Boggess does not teach or suggest that "a channel being used" in Boggess, FIG. 6A is the address of the CPU in node 2 of Boggess, FIG. 7A.

As a second example of why claim 34 is not unpatentable over Boggess in view of Floyd, Boggess Boggess in view of Floyd does not teach or suggest the feature: "sending an address of a second core and **control signals** from a first core to a first optic controller" (emphasis added). In particular, Applicants respectfully contend that Boggess does not teach or suggest that the CPU 200 sends **control signals** to the gate controller 210. The Examiner has not cited anything in Boggess to demonstrate that Boggess teaches that the CPU 200 sends control signals to the gate controller 210.

In "Response to Arguments", the Examiner argues: "Furthermore, applicant is directed to col 15, In 36-38, which describe control signal, namely the header containing the length of the data and possible some error correction scheme, are also being sent."

In response, Applicants assert that Boggess, col. 15, lines 36-38 does not teach or suggest

that the CPU 200 sends the header (alleged by the Examiner to be the control signal) to the gate controller 210. To the contrary, Boggess, col. 15, lines 31-35 teaches that the CPU ***reads*** the header. Boggess does not anywhere disclose that the CPU 200 ***sends*** the header anywhere, and Boggess most certainly does not disclose that the CPU 200 ***sends*** the header to the gate controller 210.

As a third example of why claim 34 is not unpatentable over Boggess in view of Floyd, Boggess Boggess in view of Floyd does not teach or suggest the feature: "wherein an integrated circuit comprises the first core, the first optic controller connected to the first core, a plurality of optical transmitters under control of the first optic controller, the second core, a second optic controller connected to the second core, a plurality of optical receivers under control of the second optic controller".

The Examiner argues: "Boggess further teaches a configuration of a ring topology comprising the first core *(CPU in node 1, fig 7A),* the first optic controller *(Gate Controller in fig 7A)* connected to the first core, a plurality of optical transmitters *(transmitter 240 in node 1, fig 7A)* under control of the first optic controller, the second core *(CPU in Node 2, 360, fig 7A),* a second optic controller *(gate controller in Node 2, 360, fig 7A)* connected to the second core, a plurality of optical receivers *(receivers in Node 2, 360, fig 7A)* under control of the second optic controller *(col 15, In 49-57),* and a plurality of optical channels *(channels 1-4, fig 7A),* wherein each optical channel extends from one of the optical transmitters to one of the optical receivers *(col 15, In 49-52)* ".

In response, Applicants note that all references to "the first core" after the sending step

have antecedent basis in "a first core" in the sending step of claim 34. Therefore all appearances of "the first core" in claim 34 refer to the same first core. Since the Examiner is citing the CPU 200 in Boggess, FIG. 6A as the first core in the sending step, and the Examiner is citing the CPU in node 1 in Boggess, FIG. 7A as the first core in the feature of "wherein an integrated circuit comprises the first core, ...", the Examiner's argument violates the aforementioned requirement in claim 34 that the first core must be the same first core for every appearance of the first core in claim 34.

In further response, Applicants note that all references to "the first optic controller" after the sending step have antecedent basis in "a first optic controller" in the sending step of claim 34. Therefore all appearances of "the first optic controller" in claim 34 refer to the same first optic controller. Since the Examiner is citing the gate controller 210 in Boggess, FIG. 6A as the first optic controller in the sending step, and the Examiner is citing the gate controller in Boggess, FIG. 7A as the first optic controller in the feature of "wherein an integrated circuit comprises ... the first optic controller connected to the first core, ...", the Examiner's argument violates the aforementioned requirement in claim 34 that the first optic controller must be the same first optic controller for every appearance of the first optic controller in claim 34.

As a fourth example of why claim 34 is not unpatentable over Boggess in view of Floyd, Boggess Boggess in view of Floyd does not teach or suggest the feature: "decoding, by the first optic controller, the address of the second core".

The Examiner argues the Boggess discloses "decoding, by the first optic controller, the address *(col 15, in 27-42; "... the addressing information is determined by the channel being used*

... The gate controller 210, by contrast, regulates the flow of this data over the optical interconnect, and is responsible for preventing loss of packet data due to contention for the same channels by multiple CPUs' messages. ", which means that the gate controller decodes the address by inspecting the channel being used, which determines the addressing information)".

In response, Applicants assert that the preceding quote by the Examiner of Boggess, col. 15, lines 38-42 does not teach or suggest that "the gate controller decodes the address by inspecting the channel being used, which determines the addressing information" as alleged by the Examiner. Applicants refer to Boggess, col. 17, lines 9-29 which describes how the gate controller 210 operates, and Boggess, col. 17, lines 9-29 does not teach or suggest that the gate controller 210 decodes the address of the second core.

As a fifth example of why claim 34 is not unpatentable over Boggess in view of Floyd, Boggess Boggess in view of Floyd does not teach or suggest the feature: "**after said decoding**, selecting a first optical channel of the plurality of optical channels for subsequently transmitting an optical signal over the first optical channel, wherein the first optical channel extends from a first optical transmitter of the plurality of optical transmitters and a first optical receiver of the plurality of optical receivers, and wherein said selecting is performed by the first optic controller" (emphasis added).

The Examiner argues: "after said decoding, selecting a first optical channel of the plurality of optical channels *(channels 1-4, fig 7A)* for subsequently transmitting an optical signal over the first optical channel, wherein the first optical channel extends from a first optical transmitter of the plurality of optical transmitters and a first optical receiver of the plurality of optical receivers,

and wherein said selecting is performed by the first optic controller *(col 17, In 8-15; the first gate controller send the data to the CPU if the data is in the channel that is addressed for the current node, or select a channel to forward the data to another node if it is addressed for another node.)*".

In response, Applicants assert that the preceding argument by the Examiner has not cited anything in Boggess that allegedly discloses performing the step of selecting a first optical channel **after** the step of decoding the address of the second core. In fact, Boggess does not even disclose the step of decoding the address of the second core, as explained *supra*.

As a sixth example of why claim 34 is not unpatentable over Boggess in view of Floyd, Boggess Boggess in view of Floyd does not teach or suggest the feature: "wherein an **integrated circuit** comprises the first core, the first optic controller connected to the first core, a plurality of optical transmitters under control of the first optic controller, the second core, a second optic controller connected to the second core, a plurality of optical receivers under control of the second optic controller" (emphasis added).

The preceding language in claim 34 requires that an integrated circuit (i.e., a single integrated circuit) comprises the recited structure of the first core, the first optic controller, the second core, and the second optic controller.

The Examiner acknowledges that "Boggess does not disclose expressly wherein an integrated circuit comprises the first core and the second core in a ring topology as discussed." The Examiner argues: "Floyd, from the same field of endeavor, teaches an integrated circuit comprising two cores *(paragraph 24; core 42a, 42b, fig 2),* each core is connected to a controller

(52a, 52b, fig 2; paragraph 25); Floyd further teaches a ring topology similar to that of Boggess' can be configured in one module g 3). Therefore, it would have been obvious for a person of ordinary skill in the art at the time of invention to configure Boggess' first core, first optic controller connected to the first core, a plurality of optical transmitters under control of the first optic controller, second core, a second optic controller connected to the second core, a plurality of optical receivers under control of the second optic controller, and a plurality of optical channels, wherein each optical channel extends from one of the optical transmitters to one of the optical receivers onto an integrated circuit as taught by Floyd. The motivation for doing so would have been to improve communication for system level commands to different chip components such as processor cores *(Floyd, paragraph* 11)."

In response, Applicants next demonstrate that Boggess teaches away from using a single integrated circuit.

Boggess' discussion of prior art describes disadvantages of using a single integrated circuit. For example, see Boggess, col. 2, lines 1-16 ("Due to IC packaging constraints, there is a limited electronic I/O bandwidth. According to present manufacturing techniques, an IC package can have a maximum of approximately five hundred I/O pins due to problems associated with the connections between the IC substrate and the IC package. The ... maximum I/O bandwidth of a **single IC package** is directly proportional to the number of pins times the clock rate per pin. In general, the maximum I/O bandwidth of a packaged IC is typically in the tens of Gigabits/second." (Emphasis added)).

In contrast, Boggess, col. 10, lines 63-67 teaches that for Boggess' invention: "the complexity of the control is greatly reduced as are the number of pins required to get data on and

off chip. That is, the input-output (I/O) function is distributed **across many integrated circuits** rather than trying to build one large central IC switch." (emphasis added).

Since Boggess teaches away from using a single integrated circuit, Applicants maintain that it is not obvious to modify Boggess to use a single integrated circuit instead of multiple integrated circuits.

Based on the preceding arguments, Applicants respectfully maintain that claim 34 is not unpatentable over Boggess in view of Floyd, and that claim 34 is in condition for allowance. Since claims 35-36 depend from claim 34, Applicants contend that claims 35-36 are likewise in condition for allowance.

The Examiner rejected claim 43 under 35 U.S.C. § 103(a) as allegedly being unpatentable over US Patent Number 6,674,971 to Boggess *et al.*, in view of US Patent Application Publication Number 2004/0215929 to Floyd *et al.*, as applied to claim 34 above, and further in view of US Patent Number 6,081,527 to Chappel *et al.*

Since claim 43 depends from claim 34, which Applicants have argued *supra* to not be not unpatentable over Boggess in view of Floyd under 35 U.S.C. §103(a), Applicants maintain that claim 43 is likewise not unpatentable over Boggess in view of Chappel under 35 U.S.C. §103(a).

The Examiner rejected claim 37 under 35 U.S.C. § 103(a) as allegedly being unpatentable over US Patent Number 6,674,971 to Boggess *et al.*, in view of US Patent Application Publication Number 2004/0215929 to Floyd *et al.*, as applied to claim 34 above, and further in view of US Patent Number 4,797,879 to Habbab *et al.*

Since claim 37 depends from claim 34, which Applicants have argued *supra* to not be not unpatentable over Boggess in view of Floyd under 35 U.S.C. §103(a),Applicants maintain that claim 37 is likewise not unpatentable over Boggess in view of Habbab under 35 U.S.C. §103(a).

The Examiner rejected claim 38-42 under 35 U.S.C. § 103(a) as allegedly being unpatentable over US Patent Number 6,674,971 to Boggess *et al.*, in view of US Patent Application Publication Number 2004/0215929 to Floyd *et al.*, as applied to claim 34 above, and further in view of US Patent Number 5,946,116 to Wu *et al.*

Since claims 38-42 depend from claim 34, which Applicants have argued *supra* to not be not unpatentable over Boggess in view of Floyd under 35 U.S.C. §103(a), Applicants maintain that claims 38-42 are likewise not unpatentable over Boggess in view of Wu under 35 U.S.C. §103(a).

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If the Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invites the Examiner to contact Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0456.

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Jack P. Friedman
Registration No. 44,688

Schmeiser, Olsen & Watts
22 Century Hill Drive - Suite 302
Latham, New York 12110
(518) 220-1850